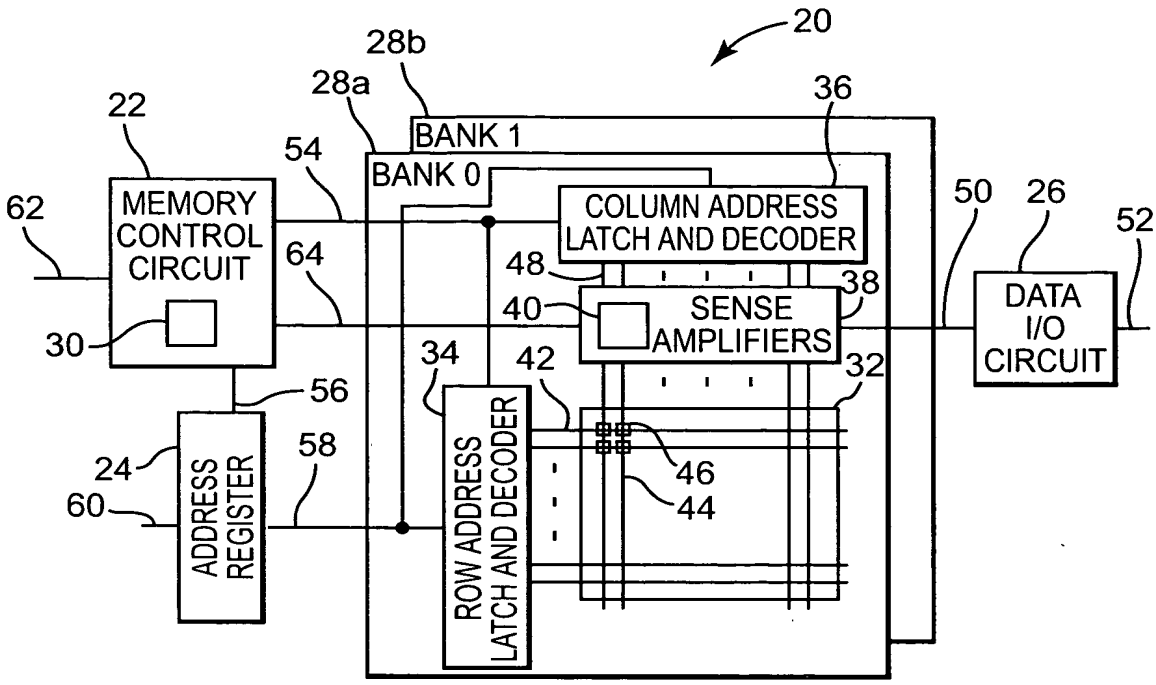
20
28b
28a
22
36
BANK 1
54
BANK 0
62
MEMORY CONTROL CIRCUIT
COLUMN ADDRESS LATCH AND DECODER
50
26
52
64
48
38
40
SENSE AMPLIFIERS
DATA I/O CIRCUIT
30
34
42
32
56
46
24
58
44
60
ADDRESS REGISTER
ROW ADDRESS LATCH AND DECODER

Fig. 1

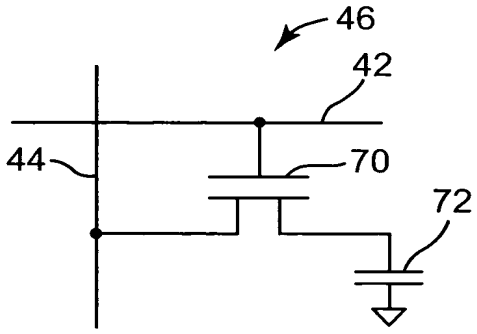
46
42
44
70
72

Fig. 2

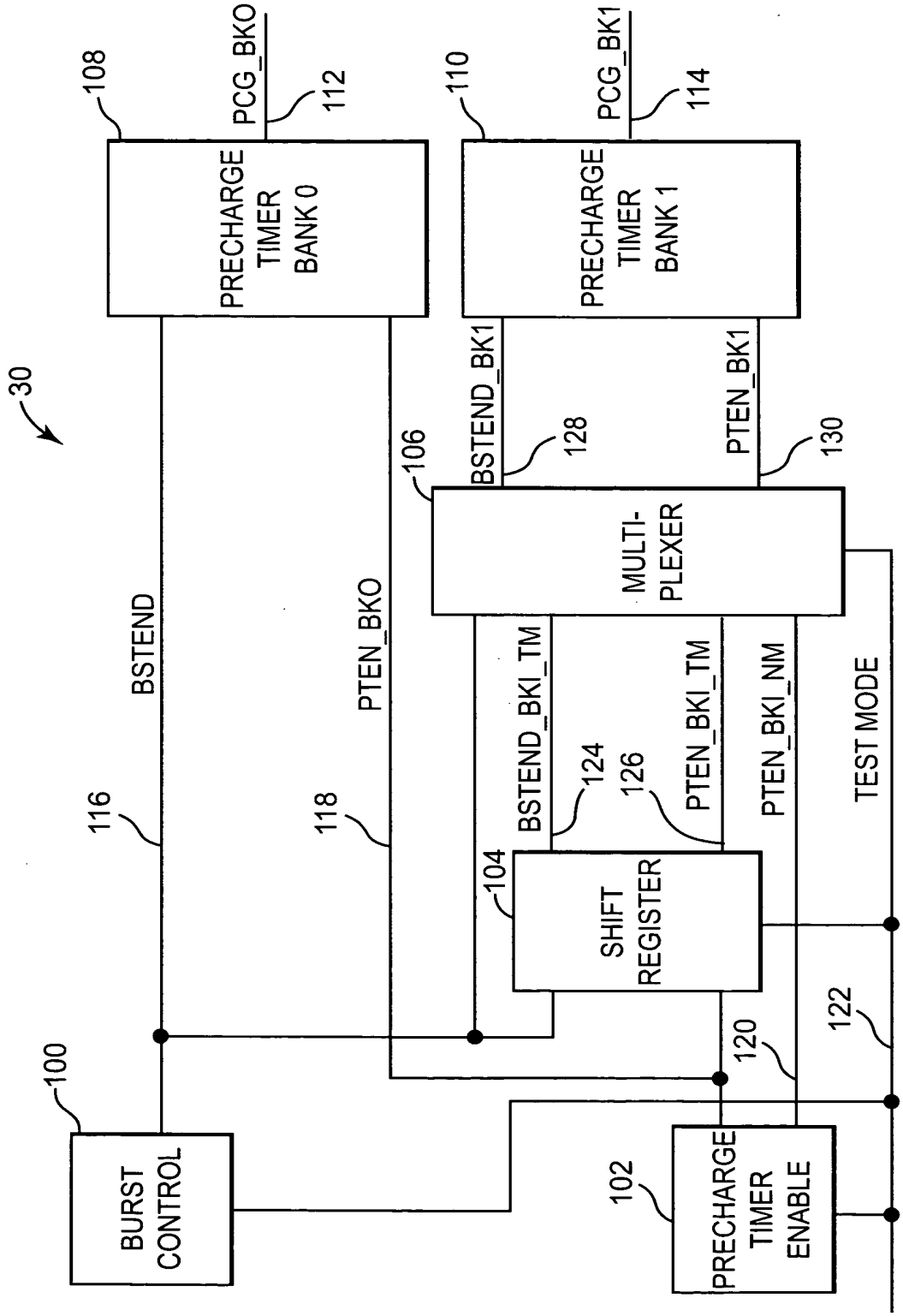
30
108
PCG_BK0
112
110
PCG_BK1
114
PRECHARGE TIMER BANK 0
PRECHARGE TIMER BANK 1
BSTEND_BK1
128
PTEN_BK1
130
106
MULTI-PLEXER
BSTEND
PTEN_BK0
BSTEND_BKI_TM
124
PTEN_BKI_TM
126
PTEN_BKI_NM
TEST MODE
116
118
104
SHIFT REGISTER
100
120
122
BURST CONTROL
102
PRECHARGE TIMER ENABLE

Fig. 3

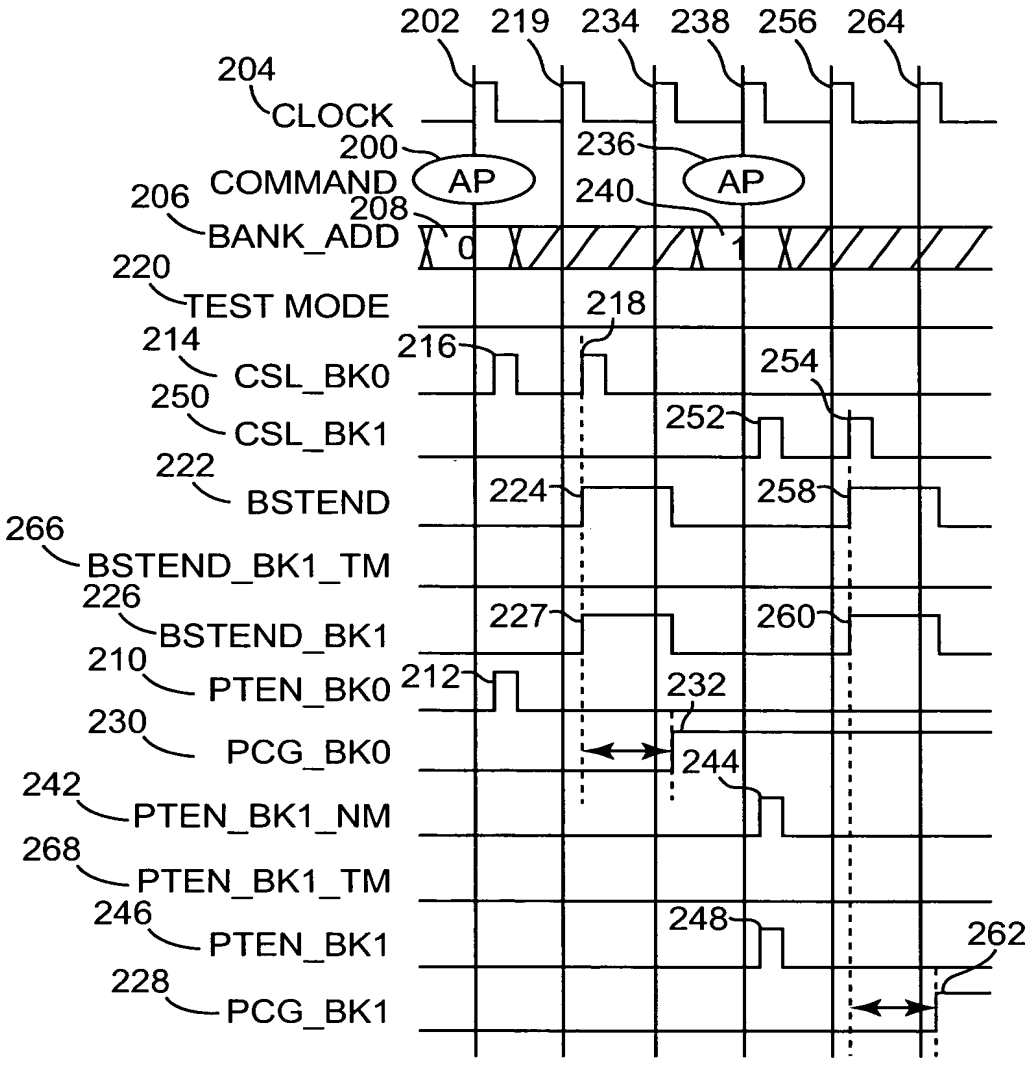
202
219
234
238
256
264
204
CLOCK
200
236
COMMAND
AP
AP
240
206
208
BANK_ADD
0
1
220
TEST MODE
218
214
216
254
CSL_BK0
250
252
CSL_BK1
222
224
258
BSTEND
266
BSTEND_BK1_TM
226
227
260
BSTEND_BK1
210
212
232
PTEN_BK0
230
PCG_BK0
244
242
PTEN_BK1_NM
268
PTEN_BK1_TM
246
248
262
PTEN_BK1
228
PCG_BK1

Fig. 4

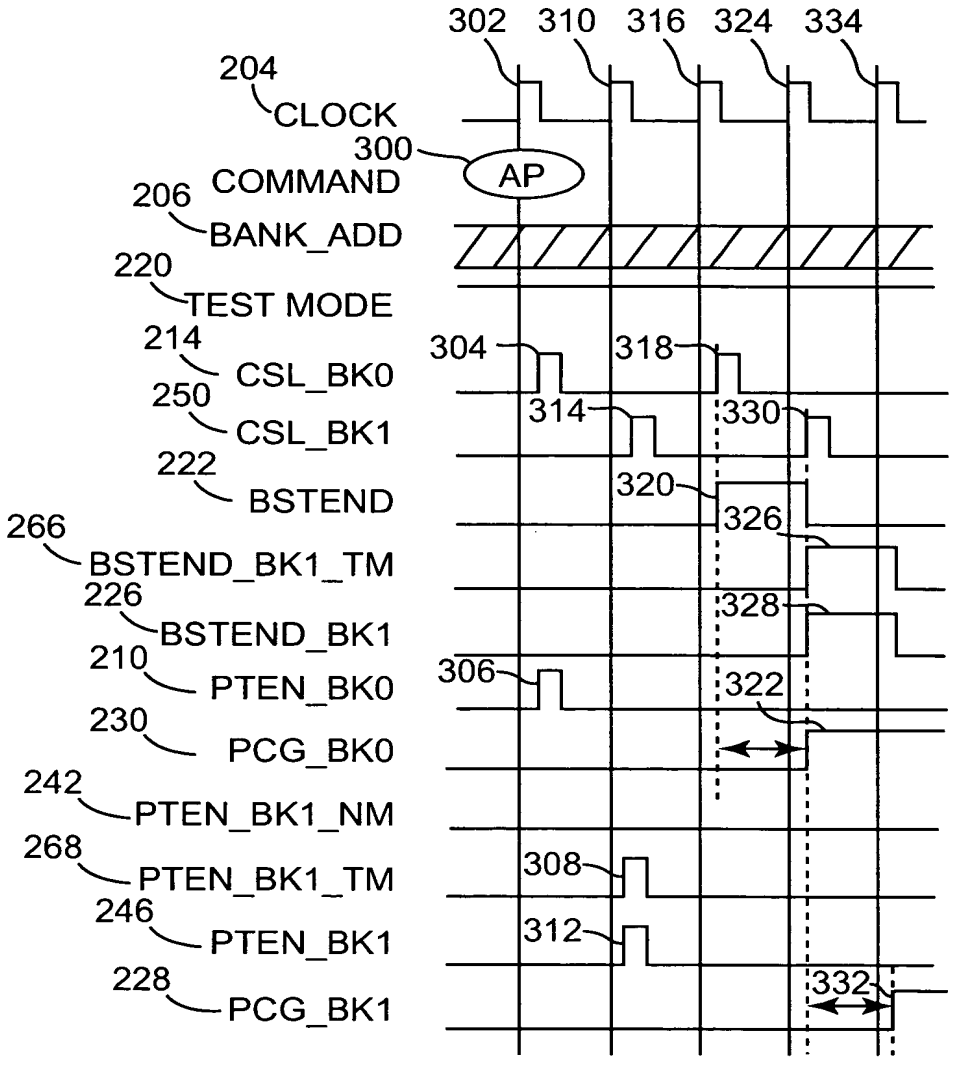
302
310
316
324
334
204
CLOCK
300
AP
COMMAND
206
BANK_ADD
220
TEST MODE
214
CSL_BK0
250
CSL_BK1
222
BSTEND
266
BSTEND_BK1_TM
226
BSTEND_BK1
210
PTEN_BK0
230
PCG_BK0
242
PTEN_BK1_NM
268
PTEN_BK1_TM
246
PTEN_BK1
228
PCG_BK1
304
318
314
330
320
326
328
306
322
308
312
332

Fig. 5